What is claimed is:

1. A method of forming a portion of a semiconductor integrated circuit; comprising the steps of:

growing a field oxide across the integrated circuit;

patterning and etching the field oxide to form an opening with substantially vertical sidewalls exposing a portion of an upper surface of a substrate underlying the field oxide where an active area will be formed;

growing a gate oxide over the exposed portion of the substrate;

depositing a polysilicon layer over the field oxide and gate oxide to a thickness wherein the lowest most portion of the upper surface of the polysilicon is above the upper surface of the field oxide;

planarizing the polysilicon layer;

forming a photoresist mask over a portion of the polysilicon layer overlying at least a portion of the substrate not covered by the field oxide;

patterning and etching the polysilicon and gate oxide to form a gate electrode;

removing the photoresist; and

forming sidewall spacers along the sides of the gate electrode.

2. The method of claim 1, wherein the field oxide has a thickness of between approximately 4000-5000 angstroms.

3. The method of claim 1, further comprising the steps of:

forming an n-well in the substrate before the field oxide is formed in areas where the field oxide will be removed.

4. The method of claim 3, wherein the n-well is formed by implantation and drive-in of phosphorous.

5. The method of claim 1, further comprising the step of:

performing a blanket implant in the substrate to adjust to desired doping levels before forming the gate oxide layer.

6. The method of claim 5, wherein the blanket implant comprises boron implanted at a dosage of approximately 1.5 X $10^{12}/cm^2$ at 30 KeV.

7. The method of claim 6, further comprising the steps of:

masking off the p-type regions; and

performing a punch-through implant into the n-well regions.

8. The method of claim 7, wherein the punch-through implant comprises boron implanted at a dosage of approximately 1 X $10^{12}/cm^2$ at approximately 75 KeV.

9. The method of claim 5, further comprising the steps of:

masking off selected p-type regions in the substrate; and

implanting dopants into selected n-wells to further adjust the doping levels of the n-wells and not the selected p-type regions in the substrate.

10. The method of claim 9, wherein the dopant comprises boron implanted at a dosage of approximately 1.7 X $10^{12}/ cm^2$ and at approximately 30 KeV.

11. The method of claim 1, further comprising the steps of:

masking off selected n-well regions in the substrate; and

implanting a dopant into the p-type regions to adjust to a desired doping level.

12. The method of claim 11, wherein the dopant comprises boron implanted at a dosage of approximately 6 X $10^{12}/cm^2$ and at approximately 180 KeV.

13. The method of claim 1, wherein the gate oxide has thickness of between approximately 70-100 angstroms.

14. The method of claim 1, wherein the polysilicon layer is formed to a thickness of between approximately 7000-9000 angstroms.

15. The method of claim 1, wherein the polysilicon is in-situ doped as deposited.

16. The method of claim 1, further comprising the step of:

doping the polysilicon to a desired doping level after deposition.

17. The method of claim 1, wherein the step of planarizing the polysilicon comprises CMP.

18. The method of claim 1, wherein the step of planarizing the polysilicon comprises the steps of:

forming a planar layer over the polysilicon layer having an etch ratio of 1:1 with the polysilicon;

performing an etchback of the planar layer and polysilicon.

19. The method of claim 18, wherein the planar layer is spin-on-glass.

20. The method of claim 18, wherein the planar layer is photoresist.

21. The method of claim 18, wherein the etchback comprises a wet etch.

22. The method of claim 18, wherein the etchback comprises chemical mechanical polishing.

23. The method of claim 18, wherein there remains a layer of polysilicon above the surface of the field oxide and in the opening after the polysilicon is etched.

24. The method claim 23, wherein the remaining polysilicon is approximately 1500-2000 angstroms over the field oxide.

25. The method of claim 18, wherein the upper surface of the polysilicon is substantially planar with an upper surface of the field oxide.

26. The method of claim 1, further comprising the step of:

forming an etch stop layer over the field oxide before the polysilicon layer is formed.

27. The method of claim 24, wherein the etch stop layer comprises nitride.

28. The method of claim 1, further comprising the step of:

forming a silicide layer over the polysilicon, the substrate and the field oxide before the photoresist is formed; and

etching the silicide with polysilicon.

29. The method of claim 28, wherein the silicide is formed from the group consisting of tantalum, tungsten, titanium and molybdenum.

30. The method of claim 28, wherein the silicide has a thickness of between approximately 1200-1700 angstroms.

31. The method of claim 1, further comprising the step of:

forming a capping layer over the polysilicon layer before the photoresist is formed; and

etching the silicide along with the polysilicon.

32. The method of claim 31, wherein the capping layer comprises oxide.

33. The method of claim 31, wherein the capping oxide has a thickness of between approximately 1200-1700 angstroms.

34. The method of claim 1, further comprising the step of:

forming lightly doped drain regions in the substrate adjacent the gate electrode before the sidewall spacers are formed.

35. The method of claim 1, further comprising the step of:

forming source/drain regions in the substrate adjacent the gate electrode after the sidewall spacers are formed.

36. The method of claim 1, further comprising the steps of:

forming a raised source/drain region adjacent the gate electrode and overlying the exposed substrate.

37. The method of claim 36, wherein the step of forming a raised source/drain further comprises the steps of:

forming a capping layer over the polysilicon layer before the photoresist is formed;

etching the capping layer with the polysilicon layer;

depositing a polysilicon layer over the transistor gate electrode, exposed substrate and the field oxide wherein the lowest most portion of the upper surface of the polysilicon layer is above the upper surface of the gate electrode;

forming a planar sacrificial layer over the polysilicon layer having a 1:1 etch rate with the polysilicon layer;

etching the sacrificial layer and the polysilicon layers exposing the upper surface of the field oxide;

doping the polysilicon layer to a desired doping level.

38. The method of claim 37, wherein the lowest most portion of the upper surface of the polysilicon layer is above the upper surface of the gate electrode.

39. The method of claim 37, further comprising the step of:

forming a silicide under the capping layer and over the polysilicon before the polysilicon is deposited.

40. The method of claim 36, wherein the step of forming a raised source/drain further comprises the steps of:

selectively growing epitaxy above the exposed substrate surface;

implanting the epitaxy with an appropriate dopant to achieve a desired conductivity level; and

siliciding an upper portion of the selectively grown epitaxy.

94... 96

41. A method of forming a portion of a semiconductor integrated circuit; comprising the steps of:

growing a field oxide across the integrated circuit;

patterning and etching the field oxide to form an opening with substantially vertical sidewalls exposing a portion of an upper surface of a substrate underlying the field oxide where an active area will be formed;

growing a gate oxide over the exposed portion of the substrate;

depositing a doped polysilicon layer over the field oxide and gate oxide to a thickness wherein the lowest most portion of the upper surface of the polysilicon is above the upper surface of the field oxide;

planarizing and etching the polysilicon layer such that the upper surface of the polysilicon layer remains at or above the upper surface of the field oxide;

forming a silicide over the polysilicon layer;

forming a capping layer over the silicide;

forming a photoresist mask over a portion of the capping layer overlying at least a portion of the substrate not covered by the field oxide;

patterning and etching the capping layer, the silicide, the polysilicon and gate oxide to form a gate electrode of a transistor;

removing the photoresist;

forming LDD regions in the substrate adjacent the gate electrode;

forming sidewall spacers along the sides of the gate electrode; and

forming source/drain regions adjacent the gate electrode.

42. The method of claim 41, further comprising the step of:

forming n-wells in the substrate before the field oxide is formed in areas where the field oxide will be removed.

43. The method of claim 41, wherein the polysilicon layer is formed to a thickness of between approximately 7000-9000 angstroms.

44. The method of claim 41, wherein the silicide is formed from the group consisting of tantalum, tungsten, titanium and molybdenum.

45. The method of claim 41, wherein the silicide has a thickness of between approximately 1200-1700 angstroms.

46. The method of claim 41, wherein the capping layer has a thickness of between approximately 1200-1700 angstroms.

47. The method of claim 41, further comprising the step of:

forming a raised source/drain region adjacent the gate electrode and overlying the exposed substrate.

94... 96

50. The structure of claim 48, further comprising:

an n-well in the active area in the substrate.

51. The structure of claim 48, wherein the gate oxide has a thickness of between approximately 70-100 angstroms.

52. The structure of claim 48, wherein the polysilicon gate electrode has a thickness of between approximately 7000-9000 angstroms.

53. The structure of claim 48, further comprising:

a silicide layer over the polysilicon gate electrode.

54. The structure of claim 53, wherein the silicide is from the group consisting of tantalum, tungsten, titanium and molybdenum.

55. The method of claim 53, wherein the silicide has a thickness of between approximately 1200-1700 angstroms.

48. A structure consisting of a portion of a semiconductor integrated circuit, comprising:

a field oxide formed across the integrated circuit having an opening therethrough with substantially vertical sidewalls exposing a portion of an upper surface of a substrate underlying the field oxide;

a gate oxide over a portion of the exposed portion of the substrate;

a polysilicon gate electrode overlying the gate oxide and having an upper surface planar with or above an upper surface of the field oxide;

LDD regions in the substrate adjacent the gate electrode; and

sidewall spacers along the sides of the polysilicon gate electrode.

49. The structure of claim 48, wherein the field oxide has a thickness of between approximately 4000-5000 angstroms.

56. The structure of claim 48, further comprising:

a capping layer over the silicide.

57. The structure of claim 56, wherein the capping layer comprises oxide.

58. The structure of claim 56, wherein the capping layer has a thickness of between approximately 1200-1700 angstroms.

59. The structure of claim 48, further comprising:

LDD regions in the substrate adjacent the gate electrode.

60. The structure of claim 48, further comprising:

source/drain regions adjacent the gate electrode in the substrate.

61. The structure of claim 48, further comprising:

raised source/drain regions adjacent the gate electrode and overlying the exposed substrate.

62. The structure of claim 61, wherein the raised source/drain regions comprise:

doped polysilicon; and

silicide over the upper surface of the doped polysilicon.

63. The structure of claim 61, wherein the raised source/drain regions comprise:

doped selectively grown epitaxy; and

silicide over an upper portion of the selectively grown epitaxy.

94... 96

64. A structure consisting of a portion of a semiconductor integrated circuit, comprising:

a field oxide formed across the integrated circuit having an opening therethrough with substantially vertical sidewalls exposing an active area in a portion of an upper surface of a substrate underlying the field oxide;

a gate oxide over a portion of the exposed substrate;

a polysilicon gate electrode overlying the gate oxide and having an upper surface planar with or above the upper surface of the field oxide;

a silicide layer over the polysilicon layer;

a capping layer over the silicide layer;

LDD regions in the substrate adjacent the gate electrode; and

sidewall spacers along the sides of the polysilicon gate electrode.

65. The structure of claim 64, further comprising:

source/drain regions adjacent the gate electrode.

66. The structure of claim 65, wherein the source/drain regions are in the substrate.

67. The structure of claim 64, wherein the source/drain regions comprise:

a raised doped polysilicon layer over the exposed substrate and adjacent to the gate electrode.

68. The structure of claim 64, wherein the source/drain regions comprise:

a raised doped selectively grown epitaxial region over the exposed substrate surface and adjacent to the gate electrode; and

a silicide over an upper portion of the epitaxial region.

Add B2

Add C1

add E27

94... 96